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**6. AUTHOR(S)**
Yashwant K. Malaiya

**7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)**
Colorado State University
Fort Collins, CO 80525

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This final report mentions the research results of this project. They are grouped into technology - specific testing, IPPQ Testing, fault modeling and testing of storage elements and arrays and reliability growth for design faults.

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# RELIABILITY MANAGEMENT THROUGH TESTING

FINAL REPORT

BMDO/IST
ONR

(1/1/1992-2/29/1996)

PI: Yashwant K. Malaiya

Colorado State University
Fort Collins CO 80523

# 1 Abstract

This objective of this project was to develop methods for achieving high reliability through testing. We looked at both technology dependent faults and design faults. Testing is used as the major approach to identify faults.

The project looked at testing at multiple levels. Some of the investigations were carried out at the transistor level. We also examined the problem of testing at the chip level where we used some of the results obtained at the lower level. The technologies examined were primarily CMOS and BiCMOS. We have taken a critical look at faults in the storage elements, which have not been examined by the researchers before. Some of the results were extended for memory systems which are arrays of storage elements. We also looked at IDDQ based testing, which is a new approach that is now receiving considerable attention.

Design faults are the primary source of software failures. They are now also becoming important for complex hardware designs. We have looked at testing based techniques for eliminating design faults as well as methods to evaluate the effectiveness of such testing.

We have obtained a number of ground-breaking results which have been reported in the literature. We expect that our work will influence not only the research being conducted at industrial or research organizations but also commercial implementations.

The research results are broadly classified in the next section.

# 2 Research Results

The related publications are indicated by the numbers as used in the list of publications below.

## 2.1 Technology Specific Testing

The major focus here has been on BiCMOS technology. In this technology, some of the limitations of CMOS are overcome by use of bipolar technology. We have identified some specific testing problems with BiCMOS. The problem of transistor level fault modeling is addressed in [2,6,22,39,41]. A new testable design for stuck-open faults is presented in [5,21]. Test generation for BiCMOS is considered in [1,3,19,24]. A new high-speed BiCMOS domino technology is presented in [7]. In addition fault modeling in ECL devices was addressed in [2,23,29].

## 2.2 IDDQ Testing

The quiescent power supply current IDDQ is very sensitive to some of the important kinds of failure modes in VLSI. IDDQ testing has now been accepted in industry and has started to play a significant role in achieving low reject rates with a limited testing time. We have examined the issues of resolution available with IDDQ testing in [12, 32]. The impact of Built-in Current sensors is evaluated in [18]. We have developed a new static memory architecture that allows high speed IDDQ testing [8,Pat.1]. It uses differential monitoring of elevated IDDQ and allows blocks to be accessed in parallel for high speed testing.

### 2.3 Storage elements/arrays

In the past only limited attention had been paid to faults within the storage elements. We have examined the affect of transistor level defects in storage elements and have shown that some of the resulting faulty behavior patters can not be modeled by existing models [2,25,29,34,40]. We have also examined fault modeling in static RAMs which are arrays of storage elements [8,9,14,30]. The papers [13,31] address testing of unclocked circuits.

### 2.4 Reliability Growth for Design faults

Some experimental software failure data has now began to become available that allows us to develop accurate models and techniques for evaluating reliability growth. The hardware verification community has started to look at software testing based techniques. Our results on reliability growth models and computational techniques have been reported in [17,26,28,36]. The papers [35,37,38,book-chapter2] report that in some cases, neural net technique can be effectively used to project software reliability. Different testing strategies can very significantly vary in effectiveness, [4,5,16,20,42,43] look at related issues. Our work on static estimation [4,20,33,42] include a new model for fault exposure ratio. A new test generation approach termed Antirandom Testing is reported in [10]. Preliminary ideas on a new integrated software tool were presented in [11]. A new model for calculating reliability using test coverage has been proposed and evaluated in [16].

## 3 Publications

### 3.1 Books/Book Chapters

1. **Bridging Faults and IDDQ Testing**, Editors: Y.K. Malaiya and R. Rajsuman, *IEEE Computer Society Press Technology Series*, 1992.

2. N. Karunanithi and Y.K. Malaiya, "Neural Networks for Software Reliability", Chapter in **Handbook on Software Reliability Enginering**, Ed. M. Lyu, Publisher: McGraw-Hill, 1996.

## 4 Patents

1. W.K. AlAssadi, A.P. Jayasumana and Y.K. Malaiya, "IDDQ Testing of Integrated Circuits" Patent application filed Oct. 24, 1996.

### 4.1 Papers

1. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "Input Pattern Classification for Detection of Stuck-on and Bridging Faults Using IDDQ Testing in BiCMOS and CMOS Circuits," Proc. International Conference on VLSI Design, Jan.1997, pp. 545-546.

2. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "ECL Storage Elements: Modeling of Faulty Behavior," to appear in IEEE Trans. Circuits & Systems.

3. S. M. Menon, A. P. Jayasumana and Y. K. Malaiya, "Input pattern classification for transistor level testing of bridging faults in BiCMOS circuits," Proc. IEEE 6th Great Lakes Symposium on VLSI, March 1996 pp. 214-219.

4. N. Li and Y.K. Malaiya, "Fault Exposure Ratio: Estimation and Applications" Proc. IEEE Int. Symp. Software Reliability Engineering 1996 pp. 372-381.

5. S.M. Menon, A.P. Jayasumana and Y.K. Malaiya "Testable Design for BiCMOS Stuck-Open Fault Detection using Single Patterns" IEEE Journal of Solid State Circuits, Aug. 1995, pp. 855-863.

6. S.M. Menon, A.P. Jayasumana and Y.K. Malaiya, "Manifestation of Faults in Single and Double BJT BiCMOS Logic Gates," Proc. IEE, Pt. E, Computers and Digital Techniques, Vol. 142, No. 2, pp. 135-144, March 1995.

7. S. M. Menon, A. P. Jayasumana and Y. K. Malaiya, "A Novel High-Speed BiCMOS Domino Logic Family," Proc. of the 1995 IEEE Intl. Symp. on Circuits and Systems (ISCAS), pp. 21-24, May 1995.

8. W.K. Al-Assadi, A.P. Jayasumana, Y.K. Malaiya, "A Bipartite Differential IDDQ Testable Static RAM Design" Proc. Int. Workshop on Memory Tech. Design and Testing, pp. 36-41, August 1995.

9. W.K. Al-Assadi, Y.K. Malaiya and A.P. Jayasumana,, "Differential IDDQ Testable Static RAM Architecture" Proc. IEEE Int. Work. on IDDQ Testing, pp. 54-59, Oct. 1995.

10. Yashwant K. Malaiya "Antirandom Testing: Getting the Most out of Black Box Testing" Proc. IEEE Int. Symp. on Software Reliability Engineering, pp. 86-95, Oct. 1995.

11. N. Li and Y.K. Malaiya "ROBUST: A Next Generation Software Reliability Engineering Tool" Proc. IEEE Int. Symp. on Software Reliability Engineering, pp. 375-380, Oct. 1995.

12. Y.K. Malaiya, A.P. Jayasumana, Q. Tong and S. Menon, "Resolution Enhancement in IDDQ testing for Large ICs" *International Journal of VLSI Design*, Vol. 1, No. 4, pp. 277-284.

13. W.K. Al-Assadi, D. Lu, A.P. Jayasumana, Y.K. Malaiya and C.Q. Tong, "Data Feed-through Faults in circuits using Unclocked Storage Elements," Electronic Letters, Vol. 30, No. 10, May 12, 1994, pp. 764-765.

14. W.K. Al-Assadi, A.P. Jayasumana, Y.K. Malaiya, "On Fault Modeling and Testing of Content Addressable Memories," Proc. Int. Memory Tech. Design and Test Workshop, Aug. 1994. pp. 78-83.

15. N. Li and Y.K. Malaiya, "On Input Profile Selection for Software Testing," Proc. Int. Symp. Software Reliability Engineering, Nov. 1994, pp. 196-205.

16. Y.K. Malaiya, N. Li, J. Bieman, R. Karcich and B. Skibbe, "The Relationship between Test Coverage and Reliability" Proc. Int. Symp. Software Reliability Engineering, Nov. 1994, pp.186-195.

17. Y.K. Malaiya and N. Li, "Software Reliability Modelling Approaches: Current Status," Proc. Int. Symp. Young Investigators on Information/Computer/Control, Beijing, Jan. 1994.

18. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, C.Q Tong, "The Effect of Built-in Current Sensors (BICS) on Operational and Test Performa nce," Proc. VLSI Design, Jan. 1994, pp.187-190.

19. S.M. Menon, A.P. Jayasumana and Y.K. Malaiya, "Input pattern Classification for Transistor Level Testing of BiCMOS Circuits" Proc. IEEE VLSI Test Symposium, 1994, pp. 457-462.

20. Y.K. Malaiya, A. von Mayrhauser and P. Srimani, "An Examination of Fault Exposure Ratio," IEEE Trans. Software Engineering, Nov. 1993, pp. 1087-1094.

21. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "Testable Design of BiCMOS Circuits for Stuck-Open Fault Detection using Single Patterns" *VLSI Test Symposium*, April 1993, pp. 296-302.

22. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "Bridging Faults in BiCMOS Circuits," Proc. 5th NASA Symp. on VLSI Design, Nov. 1993, pp. 7.1.1-7.1.10.

23. S.M. Menon, A.P. Jayasumana, Y.K. Malaiya and D.R. Clinkinbeard, "Modeling and Analysis of Bridging Faults in Emitter-Coupled Logic (ECL) Circuits," IEE Proceedings, Computer and Digital Techniques, Vol. 140, No. 4, July 1993, pp. 220-226.

24. S.M. Menon, A.P. Jayasumana and Y.K. Malaiya "Test generation for BiCMOS Circuits," *ISCAS*, May 1993, pp. 1714-1717.

25. W. Alassadi, Y.K. Malaiya and A.P. Jayasumana, "Faulty Behavior of Storage Elements and its Effects on Sequential Circuits" IEEE Trans. VLSI Systems, Dec. 1993 pp. 446-452.

26. N. Li and Y.K. Malaiya, "Enhancing Accuracy of Software reliability Prediction" Proc. IEEE Int. Symp. on Software Reliability Engineering, Nov. 1993, pp. 71-79.

27. K. Wu and Y.K. Malaiya, "A Correlated Faults Model for Software Reliability," Proc. IEEE Int. Symp. on Software Reliability Engineering, Nov. 1993, pp. 80-89.

28. A. von Mayrhauser, Y.K. Malaiya, P.K. Srimani and J. Keables, "On the Need for Simulation for Better Characterization of Software Reliability," IEEE Int. Symp. on Software Reliability Engineering, November 1993, pp. 264-273.

29. S. M. Menon, Y. K. Malaiya and Anura P. Jayasumana, "Faulty behavior of ECL Storage Elements," Proc. IEEE Int. Workshop on Memory Testing, August 1993, pp. 31-36.

30. W.K. Alassadi, Y.K. Malaiya and A.P. Jayasumana, "Modeling of Intra-Cell Defects in CMOS SRAM" Proc. IEEE Int. Workshop on Memory Testing, August 1993, pp. 78-81.

31. W.K. Alassadi, Ding Lu, A.P. Jayasumana, Y.K. Malaiya and C. Tong, "Faulty Behavior of Asynchronous Storage Elements" Proc. 5th NASA Symp. on VLSI Design, Nov. 1993, pp. 7.4.1-7.4.9.

32. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "Limitations of Built-in Current Sensors (BICS) for IDDQ Testing," IEEE Asian Test Symposium '93, Nov. 1993, pp. 243-248.

33. N. Li and Y.K. Malaiya, "Fault Exposure Ratio and Reliability Estimation" Proc. Third Workshop on Issues in Software Reliability, Nov. 1993, pp. 6.3.1-6.3 .18.

34. W. Alassadi, Y.K. Malaiya and A.P. Jayasumana, "Use of Storage Elements as Primitives for Testing Sequential Circuits," *Proc. 6th Int. Conf. on VLSI Design*, Jan. 1993, pp. 118-123.

35. N. Karunanithi, D. Whitley and Y.K. Malaiya, "Prediction of Software Reliability using a Connectionist Approach," *IEEE Trans. Software Engineering*, Sept. 1992, pp. 563-574.

36. Y.K. Malaiya, N. Karunanithi and P. Verma, "Predictability of Software Reliability Models," *IEEE Trans. Reliability*, Dec. 1992, pp. 539-546.

37. N. Karunanithi and Y.K. Malaiya, "The Scaling Problem for Neural Networks for Software Reliability Prediction" *Proc. IEEE Int. Symp. Soft. Rel. Eng.*, Oct. 1992, pp. 76-82.

38. N. Karunanithi, D. Whitley and Y.K. Malaiya, "Applying Neural Networks to Software Reliability Prediction," *IEEE Software*, July 1992, pp. 53-59.

39. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, " Single BJT BiCMOS Behavior under Stuck and Bridging Faults," *IEEE VLSI Test Symposium*, April 1992, pp. 315-320.

40. W. Alassadi, Y.K. Malaiya and A.P. Jayasumana, "Detection of Feed-Through Faults in CMOS Storage Elements," *Proc. 4th NASA Symp. on VLSI Design*, 1992, pp. 7.2.1-7.2.5.
S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "On Bridging Faults in ECL Circuits," *Proc. 5th Int. Conf. on VLSI Design*, 1992, pp. 55-60.

41. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "Behavior of Faulty Double BJT BiCMOS Logic Gates," *Proc. 4th NASA Symposium on VLSI Design*, 1992, pp. 8.4.1-8.4.12.

42. Y.K. Malaiya, A. von Mayrhauser and P. Srimani, "The Nature of Fault Exposure Ratio," *Proc. IEEE Int. Symp. Soft. Rel. Eng.*, Oct. 1992, pp. 23-32.

43. Y.K. Malaiya, A. von Mayrhauser and P. Srimani, "The Constant Per-Fault Hazard Rate Assumption," *Proc. 2nd Work. Issues in Soft. Rel. Est.*, Oct. 1992, pp. 1-5.

### 4.2 Invention Disclosures reported to CSU:

(a) "A Design for Testability scheme for detection of stuck-open faults in single BJT BiCMOS Logic devices." S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, 1992.

(b) "BiCMOS Domino: A Novel High-Speed Dynamic BiCMOS Logic Family," A.P. Jayasumana, Y.K. Malaiya and S.M. Menon, 1993

(c) W.K. AlAssadi, A.P. Jayasumana and Y.K. Malaiya, "IDDQ Testing of Integrated Circuits" Patent application filed by AMD, Oct. 24, 1996.

# 5 Technical & Professional Recognitions/Contributions by PI

## 5.1 Conferences

(a) General Chair, **The Fourth International Symposium on Software Reliability Engineering (ISSRE)**, Denver, Nov. 1993.

(b) General Chair, **Sixth International Conference on VLSI Design (VLSI Design '93)**, Bombay, India, 1993.

(c) Program Chair, **Fifth International Conference on VLSI Design (VLSI Design '92)** , Bangalore, India, 1992.

(d) General Chair, **IEEE International Workshop on IDDQ Testing (IDDQ-95)**, Washington D.C., October 1995.

(e) Chair Steering Committee, **IEEE International Workshop on IDDQ Testing**, 1996, 1997.

## 5.2 Editing (Periodicals)

- Guest editor, **IEEE Software**, Special issue on *Reliability Measurement*, July 1992, with P. Srimani.
- Guest Editor, **IEEE Design & Test** , Special issue on *VLSI Design* , Dec. 1992.
- Editor, MicroArch (-93)

## 5.3 Organizations

- Vice chair, **IEEE CS Award Committee (1995-)** (Service Awards).
- Vice Chair, **TCSE Software Reliability Engineering Committee** (-Current).
- Chair, **Test Technology TC Subcommittee on Software Testing, (1993-96).**
- **Member, Executive Committee, IEEE CS Technical Activities Board (-current); IEEE CS Conference and Tutorials Board (1994);**

## 5.4 IEEE Awards

- **IEEE CS Golden Core** Award, June 1996.
- **IEEE CS Certificate of Appreciation** Award, Oct. 20, 1996
- **IEEE CS Meritorious Service** Award, Feb. 1993.

# 6 Research Team

## 6.1 Student participants

- S. Menon, PhD (now at South Dakota School of Mines Technology)
- W. Alassadi, PhD (now at American Micro Devices, Austin TX)
- N. Li, PhD (now at Microsoft, Redmond WA)
- N. Karunanidhi, PhD (now at Bellcore, Morristown, NJ)
- K. Wu, MS (now at HP, Fort Collins CO)

## 6.2 Faculty participant

- Prof. A. P. Jayasumana, Colorado State Uni.

## 6.3 Collaborators

- R. Karcich, StorageTech
- B. Skibbe, StorageTech
- Prof. P. Srimani, Colorado State Uni.
- Prof. A. von Mayrhauser, Colorado State Uni.
- Prof. D. Whittley, Colorado State Uni.